

FIG. 1

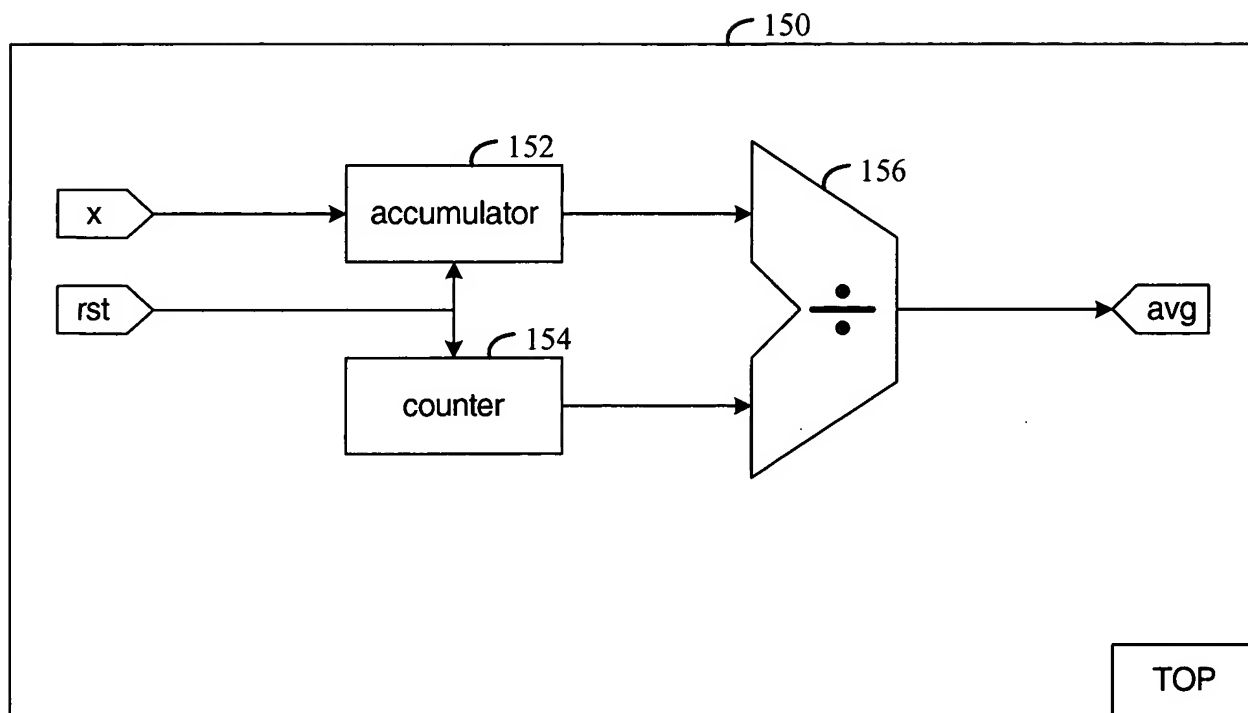


FIG. 2

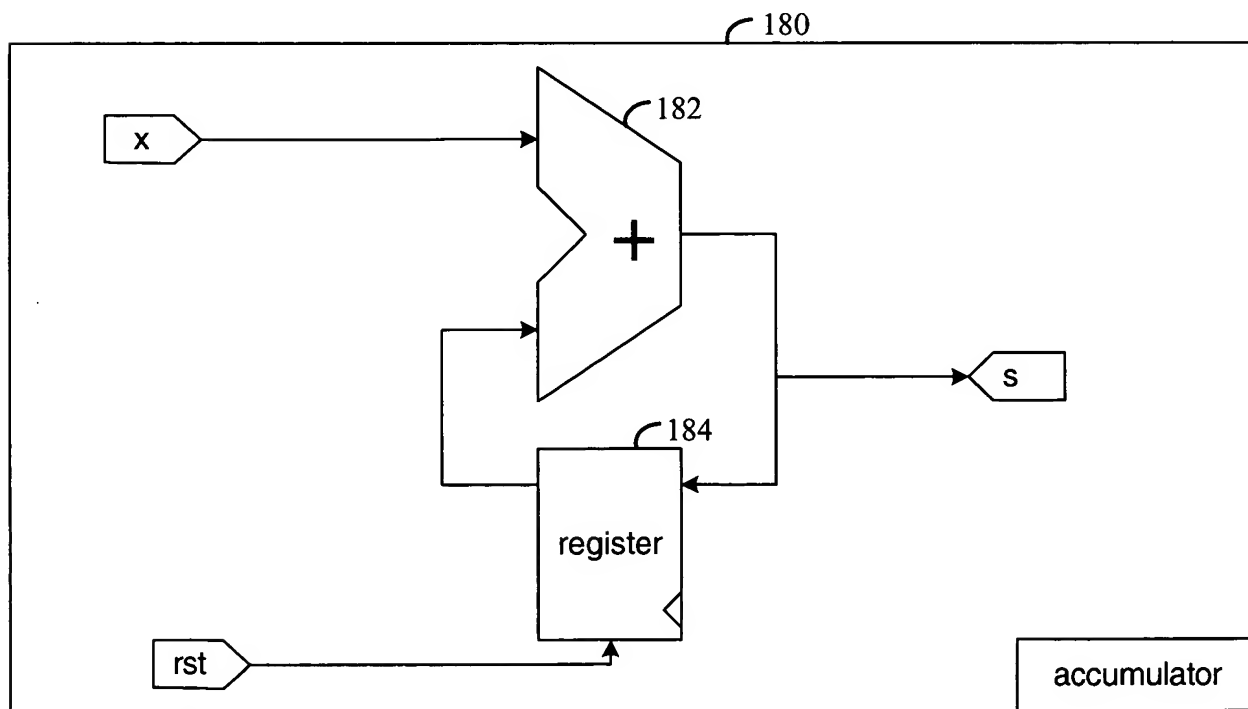


FIG. 3

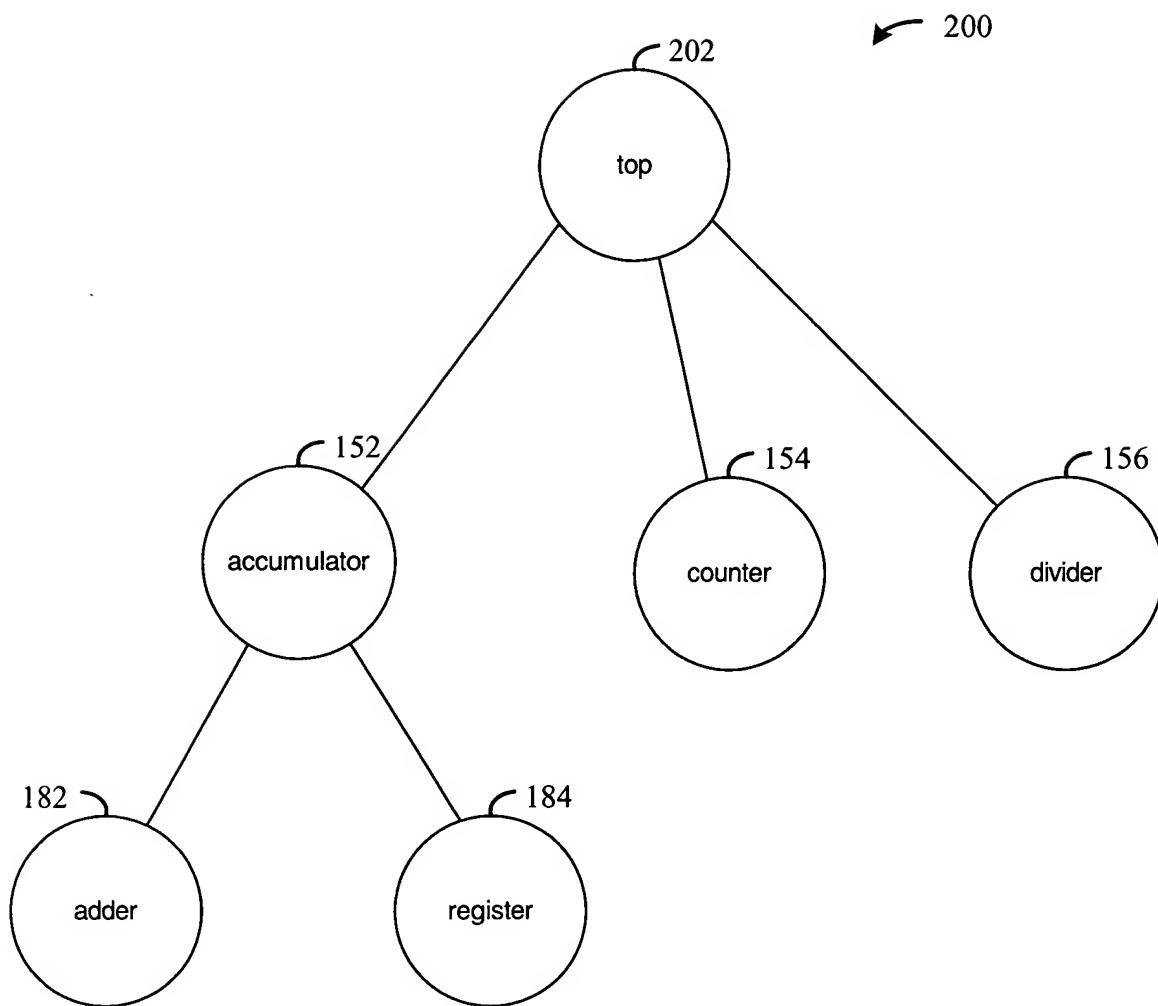


FIG. 4

250

Design-to-Hardware-Description Translation	
252	Perform necessary design-wide work on high-level blocks
254	Prepare implementers
256	$b_h :=$ top block of the HLMS design
258	Compile (b_h)
260	Complete all pending work in the implementers

FIG. 5

280

Compile (b_h)	
282	Allocate memory for a compiler block
284	Translate b_h into appropriate type of compiler block, b_k
286	If b_h has sub-blocks then
288	For each sub-block, b_i
290	Compile (b_i)
292	Implement b_k using the appropriate implementer
294	Save a lightweight description of the HDL implementation of b_k in association with the parent block of b_k
296	Free the memory of the compiler block b_k
298	Return

FIG. 6

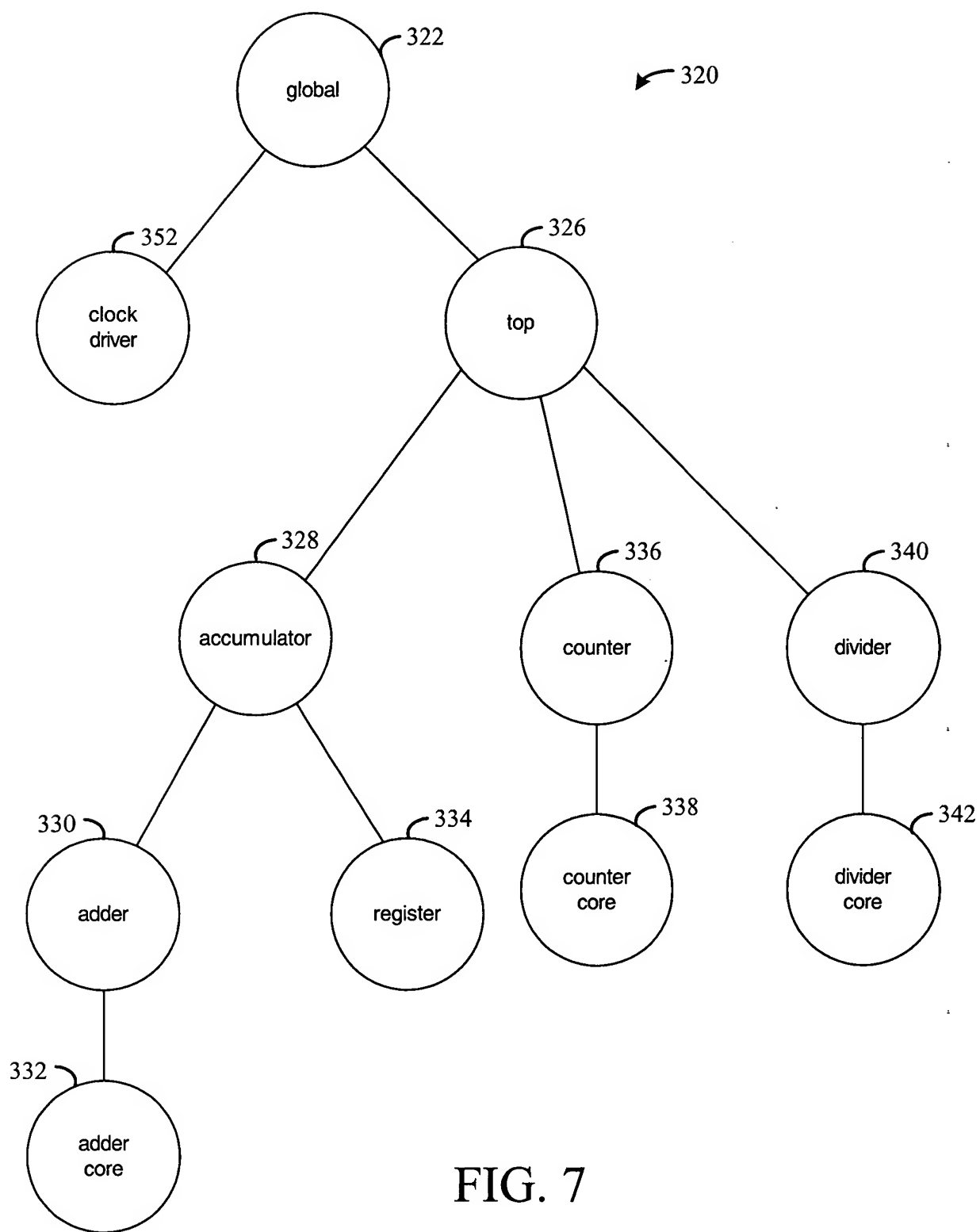


FIG. 7

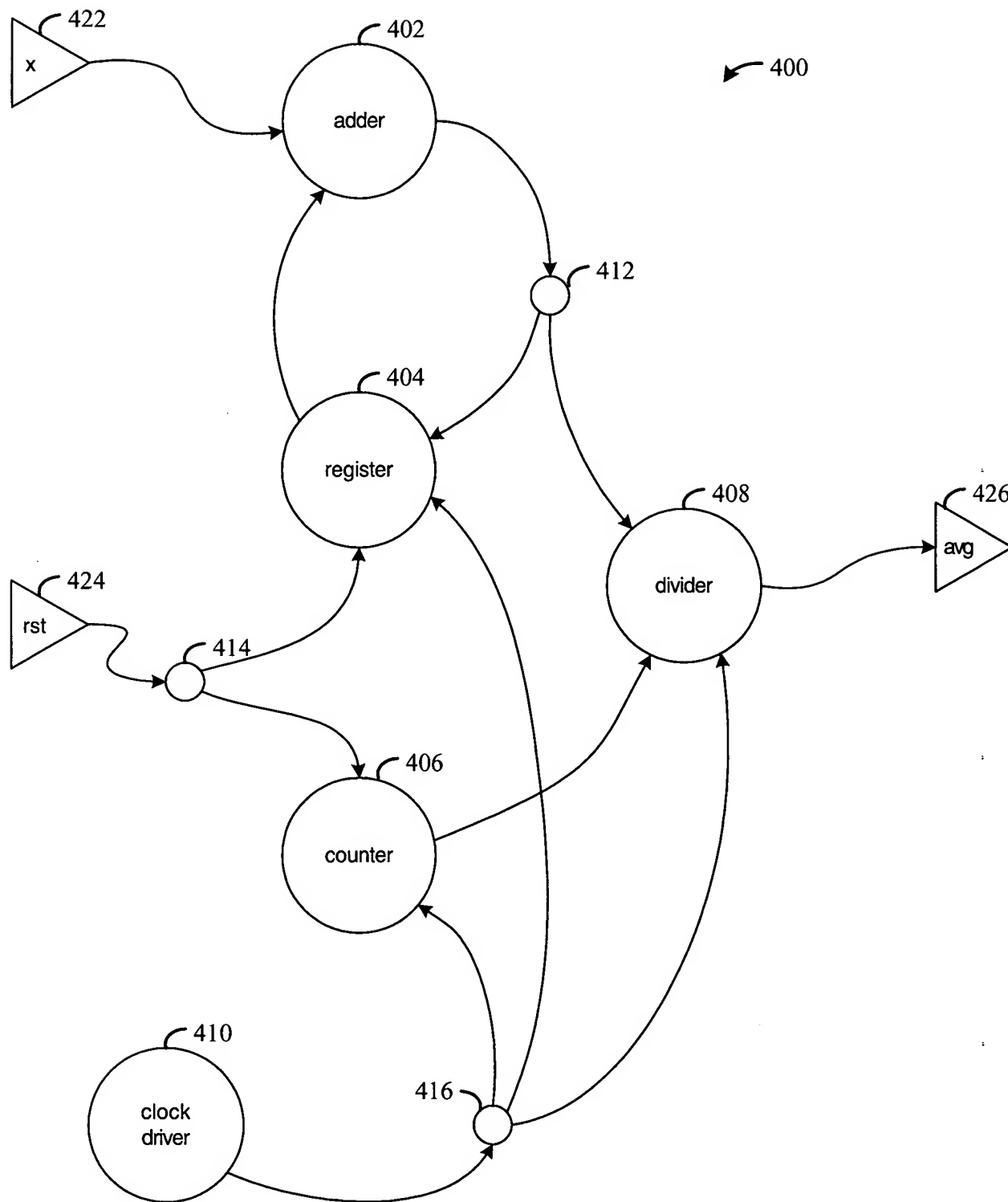


FIG. 8